

NO/PO/111/VS00

## 1 RECEIVING APPARATUS

FIG.

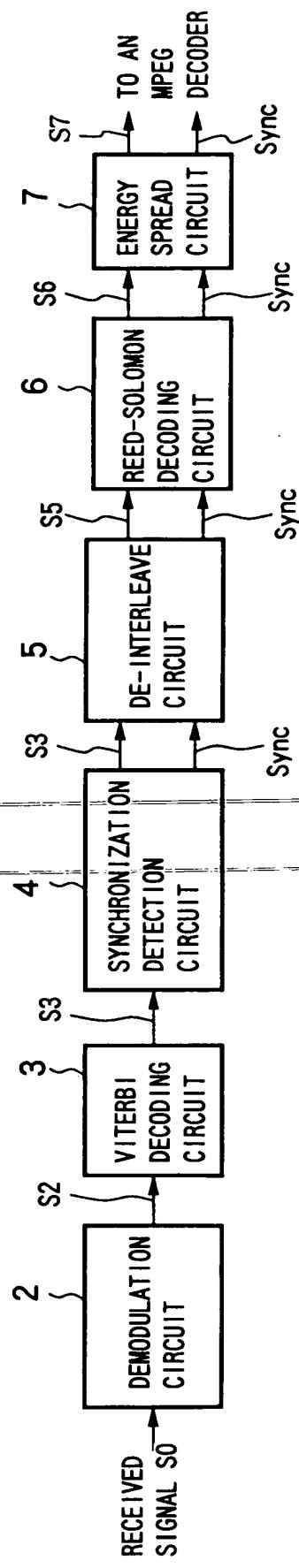
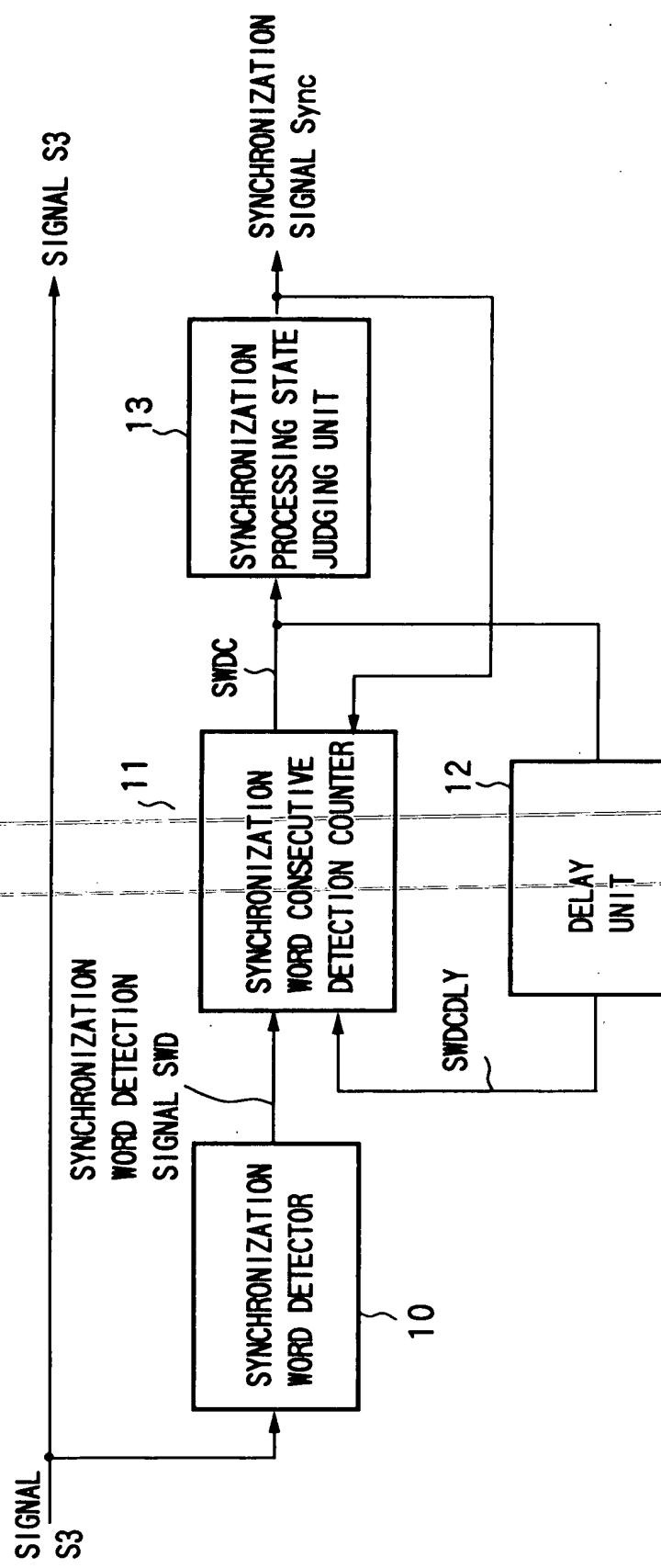
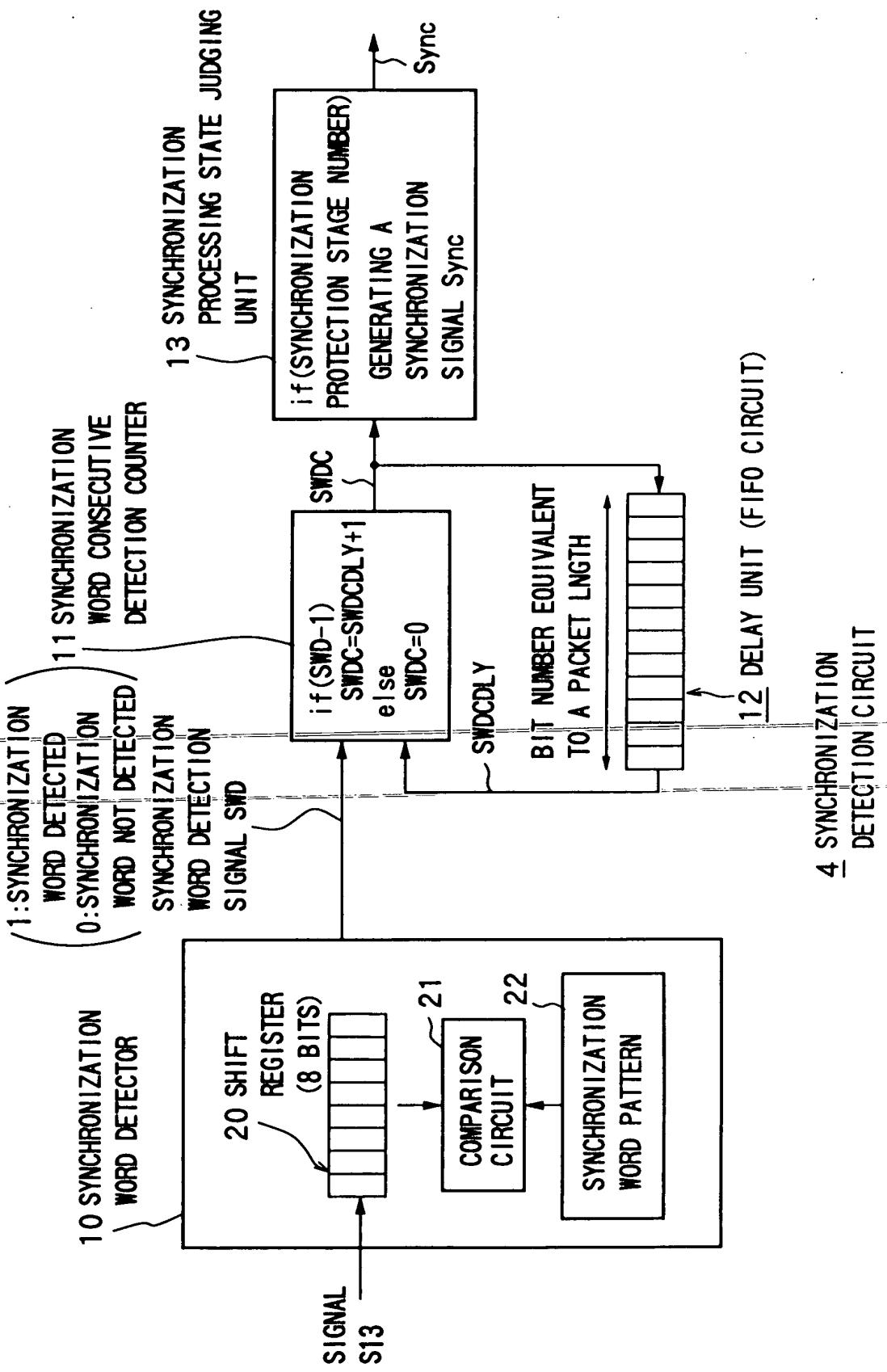


FIG.2



4 SYNCHRONIZATION  
DETECTION CIRCUIT

**FIG.3**



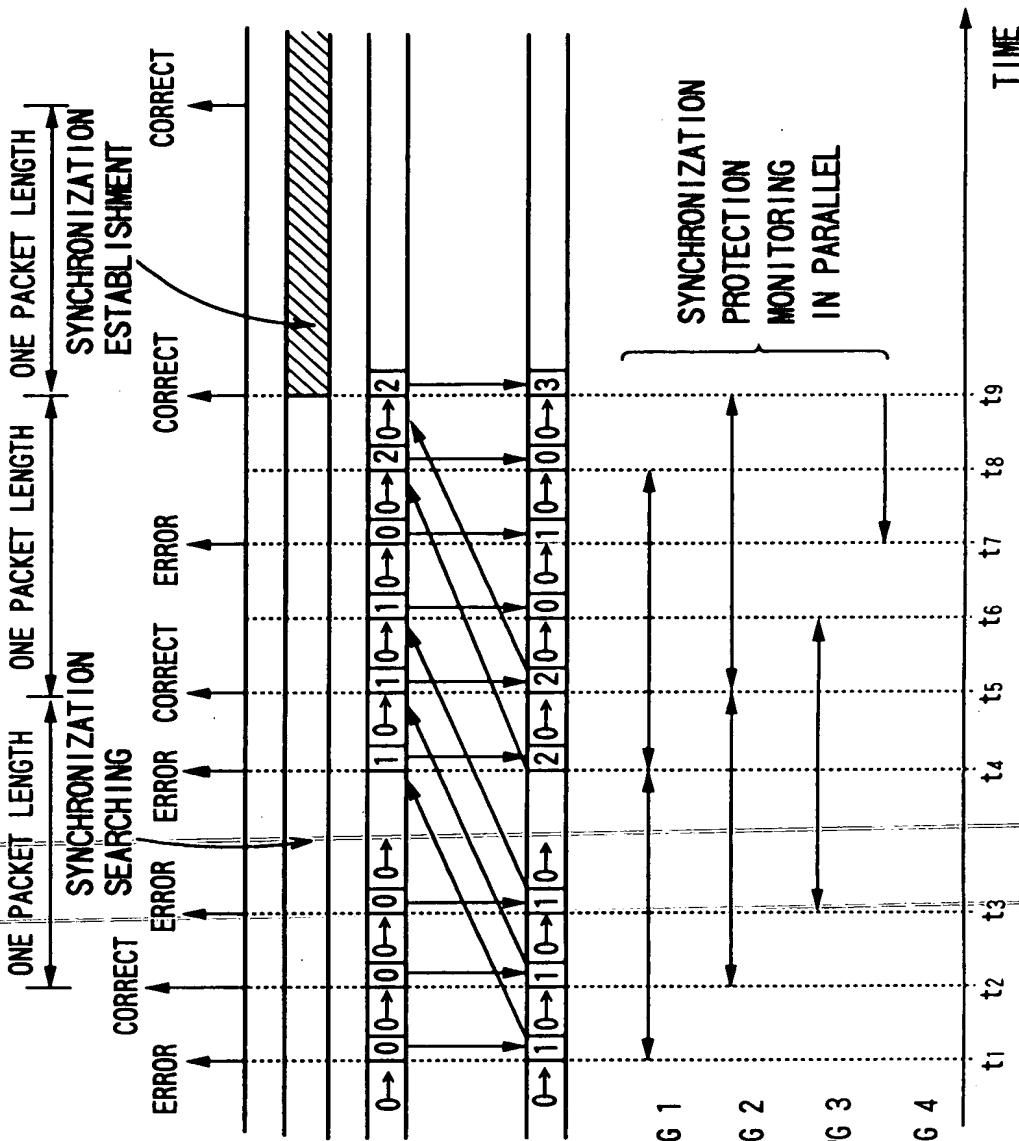


FIG.4A  
SYNCHRONIZATION  
PROCESSING STATE

FIG.4B  
SWDCDLY

FIG.4C  
SWDC

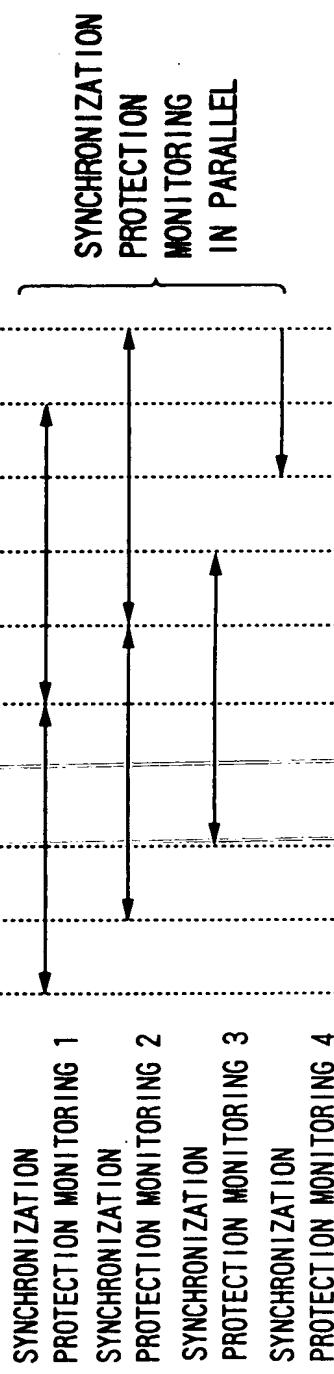
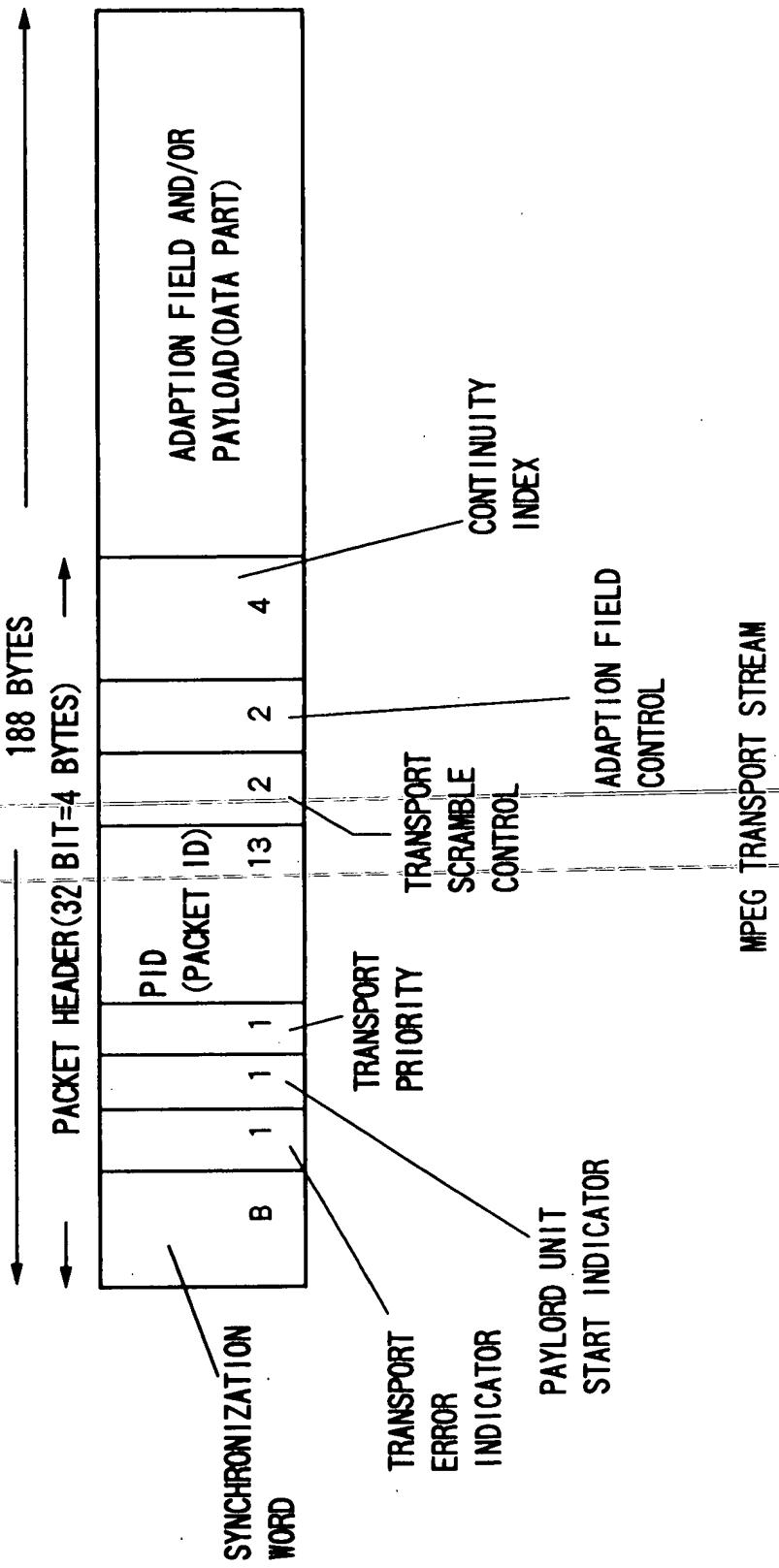
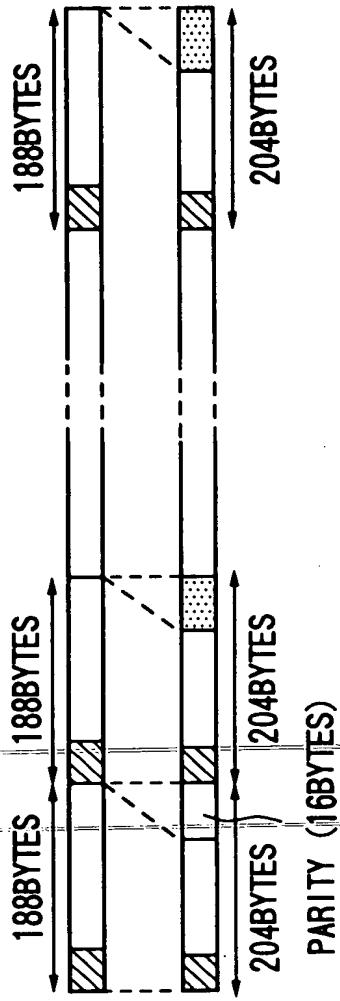


FIG.5

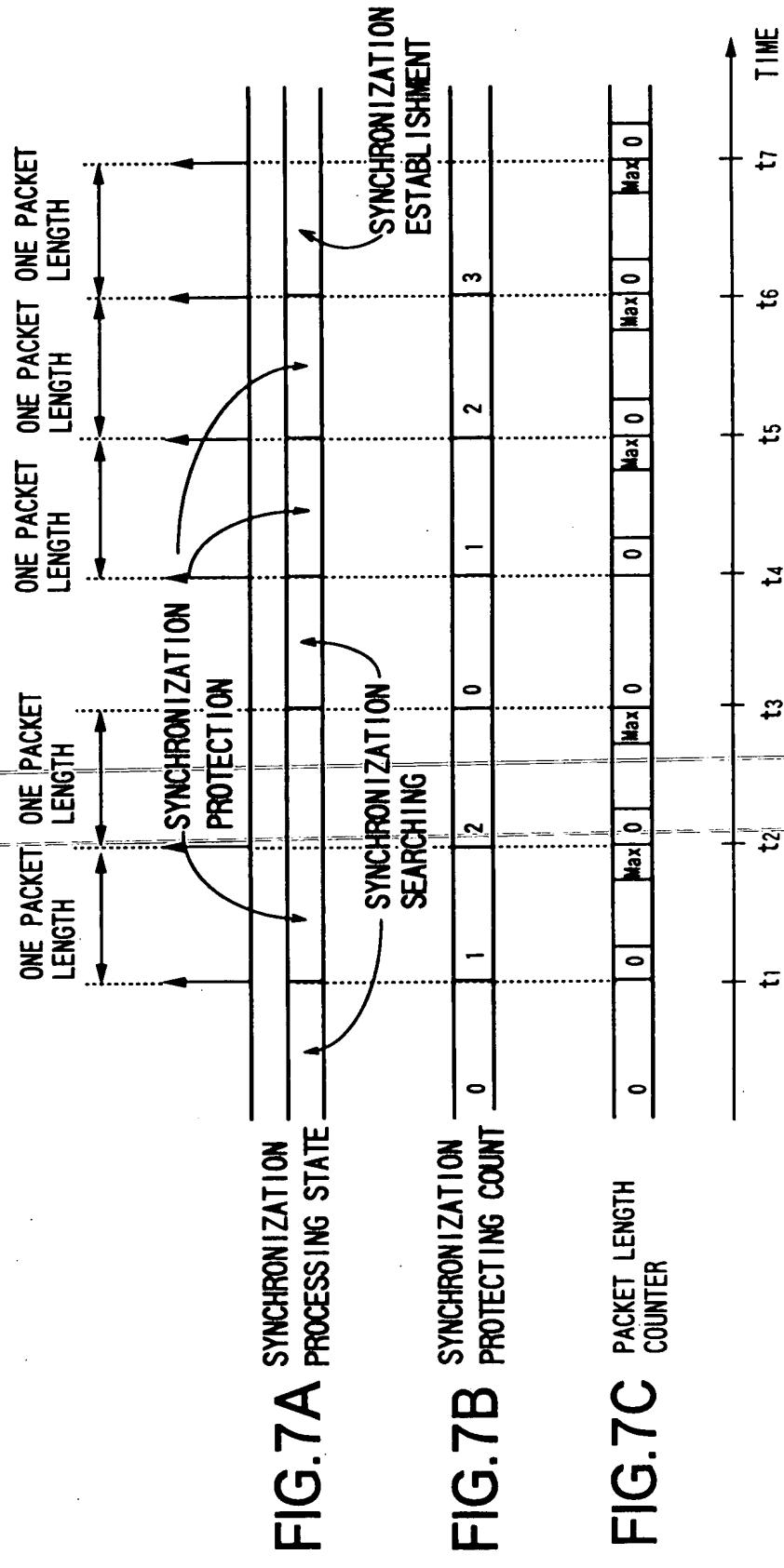


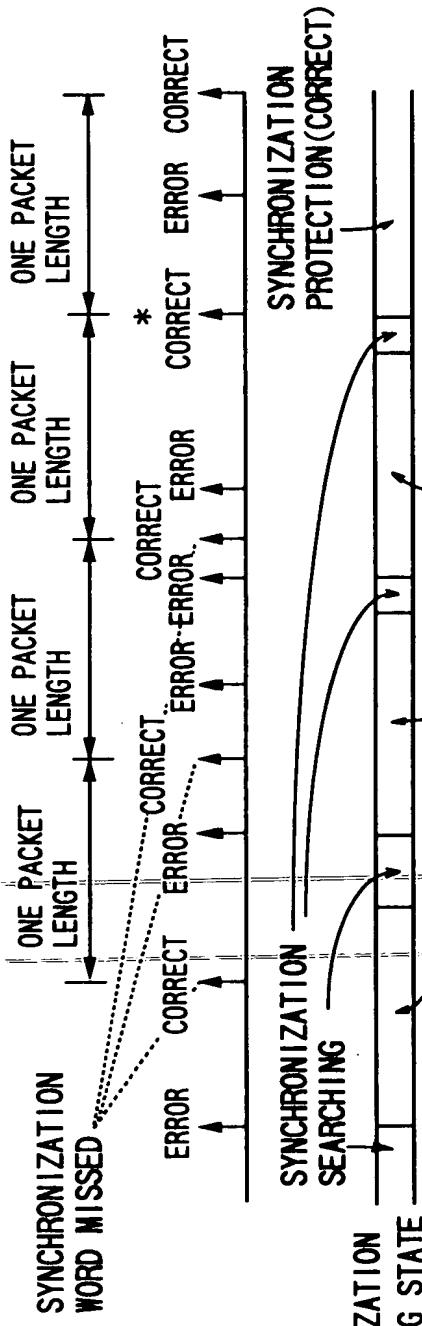
00000 = 11111 00000

**FIG.6A** TRANSPORT  
STREAM PACKET

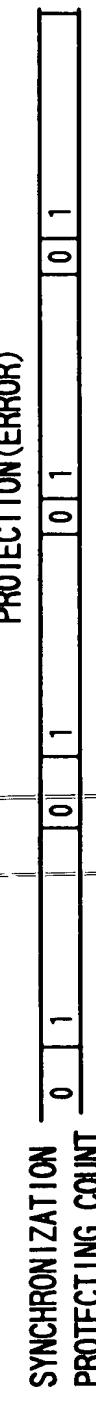


**FIG.6B** SLOT DATA

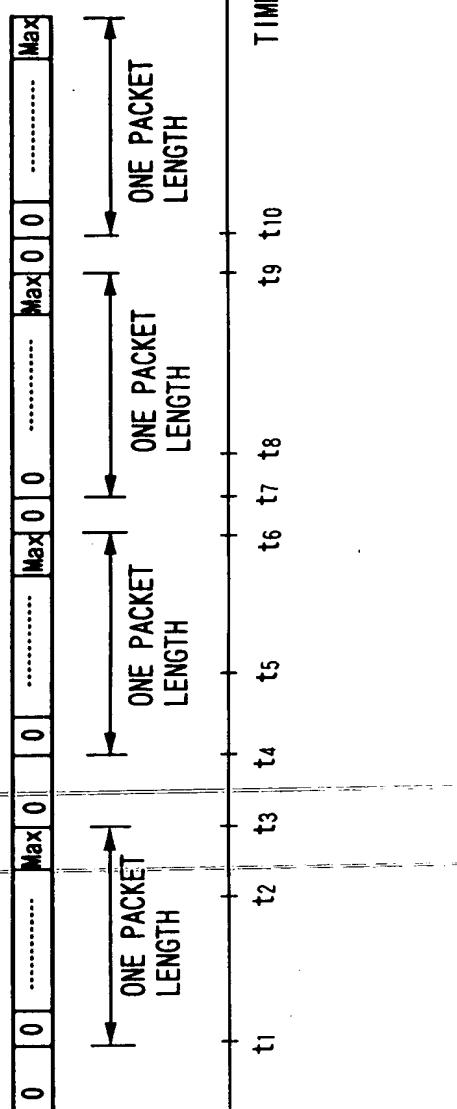




**FIG.8A** SYNCHRONIZATION PROCESSING STATE



**FIG.8B** SYNCHRONIZATION PROTECTING COUNT



**FIG.8C** PACKET LENGTH COUNTER